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| 09/986,650 | 11/09/2001 | Derek Ward | P67300US0 | 5599 |

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| EXAMINER | |
|---|---|
| JARRETT, RYAN A | |
| **ART UNIT** | **PAPER NUMBER** |
| 2125 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/986,650 | WARD, DEREK | |
| | Examiner | Art Unit | |
| | Ryan A. Jarrett | 2125 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01/22/07, 01/23/07, and 06/05/07*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *3,4,8-19 and 21-30* is/are pending in the application.

4a) Of the above claim(s) *8-19,23-26,29 and 30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,4,21,22,27 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/22/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election without traverse of claims 3, 4, 21, 22, 27, and 28 in the reply filed on 06/05/07 is acknowledged.

Claims 8-19, 23-26, 29, and 30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 06/05/07.

### *Priority*

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in New Zealand on 11/9/00. It is noted, however, that applicant has not filed a certified copy of the foreign application as required by 35 U.S.C. 119(b).

### *Information Disclosure Statement*

The information disclosure statement (IDS) submitted on 01/22/07 was in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

***Claim Objections***

Claims 3 and 4 are objected to because of the following informalities:

Claim 3 recites the limitation "said user program circuit" in lines 15 and 18. There is no explicit antecedent basis for these limitations. It appears that these limitations should be changed to "said user control program circuit".

Claim 3 recites the limitation "said programmable logic" in line 17. There is no explicit antecedent basis for this limitation. Does Applicant intend for this to read "said programmable logic hardware"?

Claim 4 recites the limitation "said programmable logic circuit" in line 5. There is no explicit antecedent basis for this limitation. Does Applicant intend for this to read "said programmable logic hardware"?

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3, 4, 21, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by "Virtex-E 1.8 V FPGAs: Preliminary Product Specification". Xilinx (9/20/00) DS022 v1.7. (hereinafter referred to as "Virtex-E")

For example, per claim 3, Virtex-E discloses an FPGA in which a monitoring device may be connected via said means of access to said state data storage units, and said means of access to said state data storage units enables said monitoring device to read data values from said state data storage units and to write data values to said state data storage units while the user control program continues to perform control functions (e.g., pg. 19: "Readback", pg. 14: "For in-circuit debugging, an optional download and readback cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.").

Per claim 4, Virtex-E discloses a logic processing interval (e.g., pg. 14: "single-step the logic") in sequence with a data access interval (e.g., pg. 14: "readback the contents of the flip-flops").

Per claims 21 and 22, Virtex-E discloses reading back the contents of the flip-flops to observe the internal logic state.

Claims 3, 4, 21, 22, 27, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by New et al. US 6,091,263.

For example, per claims 3 and 4, New et al. discloses an FPGA in which a monitoring device may be connected via said means of access to said state data storage units, and said means of access to said state data storage units enables said monitoring device to read data values from said state data storage units and to write data values to said state data storage units while the user control program continues to perform control functions (e.g., pg. 10 lines 18-39).

Per claims 21 and 22 (see e.g., col. 3 line 66 – col. 4 line 10, col. 4 lines 58-65)

Per claims 27 and 28 (see e.g., e.g., col. 8 line 13 – col. 10 line 30)

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Virtex-E as applied to claim 22 above, and further in view of New et al. US 6,091,263.

Virtex-E does not appear to explicitly disclose means to support relocation of state data during a program swap operation.

New et al. discloses a rapidly reconfigurable FPGA comprising means to support relocation of state data during a program swap operation, as recited in claims 27 and 28 (e.g., col. 8 line 13 – col. 10 line 30).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Virtex-E with New et al. since New et al. teaches that enabling state data values to be saved and restored from different local cache memories advantageously expands the configuration and reconfiguration possibilities of the configurable logic block (col. 9 lines 7-10).

***Response to Arguments***

Applicant's arguments, see pages 15-17, filed 01/22/07, with respect to rejection of claims 17-19 and 21-27 under 35 U.S.C. 112 1st paragraph (new matter) have been fully considered and are persuasive. The rejection of claims 17-19 and 21-27 under 35 U.S.C. 112 1st paragraph (new matter) has been withdrawn.

Applicant's arguments, see pages 18-28, filed 01/22/07, with respect to the rejection of claims 3, 4, 8, 9, 17-19, and 21-27 under 35 U.S.C. 102(b) as being anticipated by Vasko (US 6,463,339) have been fully considered and are persuasive. The rejection of claims 3, 4, 8, 9, 17-19, and 21-27 under 35 U.S.C. 102(e) as being anticipated by Vasko (US 6,463,339) has been withdrawn.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan A. Jarrett whose telephone number is (571) 272-3742. The examiner can normally be reached on 10:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan A. Jarrett
Primary Examiner
Art Unit 2125

09/01/07